Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("6088263").PN.	US-PGPUB; USPAT	OR	OFF	2005/12/13 13:58
L2	43	(ting adj wah and wong)	US-PGPUB; USPAT	OR	ON	2005/12/13 14:04
L3	17	2 and @ad<"19991115"	US-PGPUB; USPAT	OR	ON	2005/12/13 14:23
L4	16	3 and (floating)	US-PGPUB; USPAT	OR	ON	2005/12/13 13:59
L5	14	(ting adj wah and wong)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 14:21
L6	459	((floating adj gate) and (control adj gate) and drain and source and mask and (doping or implanting or implantation)).clm.	US-PGPUB; USPAT	OR	ON	2005/12/13 14:23
L7	204	6 and @ad<"19991115"	US-PGPUB; USPAT	OR	ON	2005/12/13 14:23

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	206	((floating adj gate) and (control adj gate) and drain and source and mask and (doping or implanting or implantation)) and (triple near3 wells)	US-PGPUB; USPAT	OR	ON	2005/12/13 15:57
L2	71	1 and @ad<"19991115"	US-PGPUB; USPAT	OR	ON	2005/12/13 15:57

US-PAT-NO: 6114724

DOCUMENT-IDENTIFIER: US 6114724 A

TITLE: Nonvolatile semiconductor memory cell with select gate

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Abstract Text - ABTX (1):

An electrically erasable programmable read only memory (EEPROM) cell including a tunnel dielectric layer formed over a semiconductor substrate. The EEPROM cell may have a floating gate transistor and a select transistor. The floating gate transistor may have a floating gate formed over the tunnel dielectric and a **control gate** formed over the floating gate. The select transistor may have a first gate formed over the tunnel dielectric and a second gate formed over the first gate. The second gate may be electrically connected to the first gate.

Brief Summary Text - BSTX (5):

A cross-section of a typical conventional EEPROM cell 100 is shown in FIG. 1A. EEPROM cell 100 is formed on semiconductor substrate 102 and includes a select transistor 124 and a floating gate transistor 122. Select transistor 124 includes **source** region 106, **drain** region 108, gate oxide 112 and select gate 116. Floating gate transistor 122 includes **source** region 104, **drain** region 106 (which it shares with select gate 106), tunnel oxide 110, floating gate 118, interlayer dielectric 114, and **control gate** 120. Erasing of floating gate transistor 122 is typically accomplished by storing negative charge on floating gate 118. This may be accomplished by applying a large positive voltage to **control gate** 120 and grounding regions 104 and 106 such that electrons may tunnel through tunnel oxide 110 to floating gate 118. Programming of floating gate transistor 122 may be accomplished by applying a large positive voltage to select gate 116 (e.g., 15-20 volts), applying a large positive voltage to **drain** region 108, applying ground to **control gate** 120, and floating **source** region 104. In this configuration, electrons may tunnel from floating gate 118 to region 106 through tunnel dielectric 118 to create a positive charge on floating gate 118.

Brief Summary Text - BSTX (8):

Another disadvantage of EEPROM cell 100 is that the size is generally large due to the high positive voltage applied to select gate 116 for programming.

The high positive voltage typically requires that the channel region of select transistor 124 (i.e., between regions 106 and 108) be increased to avoid punch-through of the region. This generally negatively impacts the speed of EEPROM cell 100. The cell size may also be generally large due to the formation of **control gate** 120 over floating gate 118. **Control gate** 120 is typically formed over floating gate 118 after regions 104 and 106 are formed. Thus, lateral diffusion of regions 104 and 106 that occurs when forming layer 114 or **control gate** 120 may be significant and may lead to punch-through problems. The channel region between regions 104 and 106 is typically increased to reduce the likelihood of punch-through problems. **Control gate** 120 is also typically formed to overlap each side of floating gate 118 by a certain amount to account for alignment tolerances between layers. Due to minimum spacing requirements between features in a particular process, this also generally increases the size of EEPROM cell 100.

Brief Summary Text - BSTX (9):

FIG. 1B shows EEPROM cell 100 formed in another conventional manner with tunnel oxide 110 forming a tunnel window 111 over region 106. The cell size is generally increased in FIG. 1B by forming tunnel window 111 over region 106. This is generally due to allowance of processing and lithographic alignment tolerances in forming tunnel window 111 after region 106 which tends to increase the length of region 106. Additionally, select transistor 124 typically requires additional graded **source and drain** junctions so as to pass high voltages, and long effective channel lengths to prevent **drain to source** punch through when select transistor 124 is off. This tends to increase the processing complexity and size of cell 100. A top view of FIG. 1B is shown in FIG. 1C.

Brief Summary Text - BSTX (13):

One embodiment of the present invention concerns an electrically erasable programmable read only memory (EEPROM) cell including a tunnel dielectric layer formed over a semiconductor substrate. The EEPROM cell may have a floating gate transistor and a select transistor. The floating gate transistor may have a floating gate formed over the tunnel dielectric and a **control gate** formed over the floating gate. The select transistor may have a first gate formed over the tunnel dielectric and a second gate formed over the first gate. The second gate may be electrically connected to the first gate.

Drawing Description Text - DRTX (9):

FIG. 3B is a cross-sectional view of an EEPROM cell formed in a **triple-well** process according to one embodiment of the present invention;

Detailed Description Text - DETX (3):

As will be described in more detail below, one embodiment of the present invention concerns an electrically erasable programmable read only memory (EEPROM) cell including a tunnel dielectric layer formed over a semiconductor substrate. The EEPROM cell may have a floating gate transistor and a select transistor each formed over the tunnel dielectric. This may avoid additional process steps of forming two gate oxide thicknesses. This may also generally allow for the use of low programming voltages to be supplied to the select transistor. The floating gate transistor may have a floating gate formed over the tunnel dielectric and a **control gate** formed over the floating gate with an interpoly dielectric separating the two gates. The select transistor may have a first gate formed over the tunnel dielectric and a second gate formed over, and electrically connected to, the first gate. The select gate and floating gate transistors may be formed from a double-poly self-aligned stacked gate technology. This may reduce complexity of forming the EEPROM cell, and may reduce the size of the EEPROM cell relative to conventional EEPROM cells. Additionally, an improved decoding scheme is disclosed that may be used to provide appropriate programming, erasing, and reading voltages to selected (and deselected) EEPROM cells in an EEPROM array.

Detailed Description Text - DETX (4):

FIG. 3A is a cross-sectional view of one embodiment of an EEPROM cell 300 according to the present invention. EEPROM cell 300 includes a floating gate transistor 326 and a select or isolation transistor 328 formed over semiconductor substrate 302. Semiconductor substrate 302 may be a P-type substrate. Alternatively, substrate 302 may be an N-type. Floating gate transistor 326 includes a floating gate 314 formed over a tunnel dielectric layer 310, and a **control gate** 322 formed over an interlayer dielectric 318. Floating gate 326 may store data for memory cell 300. Floating gate transistor 326 also includes a **source** region 304 and a **drain** region 306 each formed in substrate 302. Select gate 328 includes a first gate 316 formed over a tunnel dielectric layer 312, and a second gate 324 formed over interlayer dielectric 320. Select gate transistor 328 also includes a **drain** region 308, and a **source** region 306 that it may share with the **drain of floating gate** transistor 326. First gate 316 and second gate 324 may be electrically connected together (not shown in FIG. 3A) so as form one electrical gate that may be used to control access to floating gate transistor 326. Regions 304, 306, and 308 may be doped N+ regions when substrate 302 is a P-type substrate. Alternatively, regions 304, 306, and 308 may be P+ regions when substrate 302 is an N-type substrate.

Detailed Description Text - DETX (5):

Cell 300 may be formed in a **triple-well** process as shown in FIG. 3B. FIG.

3B shows that substrate 302 includes N-well 307 and P-well 305. Cell 300 may be formed in P-well 305. P-well 305 may be taken to negative voltages. In an alternative embodiment, regions 304, 306, and 308 may be P-type regions, substrate 302 may be N-type, well 305 may be N-type, and well 307 may be P-type.

Detailed Description Text - DETX (7):

Floating gate transistor 326 and select transistor 328 may be formed from a double-poly self-aligned stacked process as described below. This process may enable tunnel oxide layers 310 and 312 to be formed from the same layer of oxide, floating gate 314 and first gate 316 to be formed from the same layer of conductive material (e.g., a first polysilicon layer), and **control gate** 318 and second gate 324 to be formed from the same layer of conductive material (e.g., a second polysilicon layer). This may reduce the number of process steps required to form EEPROM cell 300 when compared with conventional EEPROM cells.

Detailed Description Text - DETX (11):

As shown in FIG. 6, layers 502, 504, 506, and 508 may be patterned to form two self-aligned stacks corresponding to floating gate transistor 326 and select transistor 328. The patterning process may be any conventional lithography process, or any other process for selectively removing regions of layers 504, 506, 508, and/or 502 to create the stacks illustrated in FIG. 6. For example, photoresist may be deposited over second conductive layer 508 and selectively exposed to light or radiation and developed to create a **mask** over those portions that may subsequently form **control gate** 322 and second gate 324. The regions surrounding the stacks may then be etched and the photoresist removed from **control gate** 322 and second gate 324. Doped regions 304, 306, and 308 may then be formed by ion **implantation** or other known **doping** techniques. Regions 304, 306, and 308 may include any suitable type of N-type **doping** material including phosphorus, arsenic, and the like. Additionally, and/or alternatively, region 306 (and/or regions 304 and 308) may be formed as graded junctions to reduce the electric field between region 302 and region 306. A graded junction may be formed by forming a region of N- **doping** material in addition to forming the N+ material in region 306. The N- dopant may be Phosphorus which may be implanted at an angle to place it in front of the N+ material which may be Arsenic. Junction grading can also result from a high temperature drive step since Phosphorous typically diffuses faster and ahead of Arsenic. A graded junction may further reduce the channel region under tunnel dielectric layer 310 which may result in increased speed and reduced current flow into substrate 302. Additionally, the angle of **implantation for implanting** the N+ material into region 306 (and/or regions 304 and 308) may be controlled so as to control the amount of lateral diffusion of region 306

(and/or regions 304 and 308) that occur due to subsequent process steps. FIG. 7 shows EEPROM cell 300 after regions 304, 406, and 308 have laterally diffused due to subsequent process steps. The lateral diffusion may further reduce the channel regions underlying the stacks.

Detailed Description Text - DETX (13):

8. **Control gate** 322 is shown overlying floating gate 314, and second gate 324 is shown overlying first gate 316. First gate 316 and floating gate 314 are shown as broken diagonal lines.

Detailed Description Text - DETX (15):

Control gate 322 may be formed to be narrower than conventional **control gates**. The same patterning step used to form **control gate** 322 may be used to define floating gate 314 by etching the stack formed by layers 322, 318, and 314. Thus, as opposed to conventional fabrication techniques, **control gate** 322 does not need to extend beyond the length of floating gate 314 to account for alignment tolerances. The select gate layers 324, 320, and 316 are also defined by self-aligned stack etch during the same patterning step.

Detailed Description Text - DETX (16):

With respect again to FIG. 4, one embodiment of the geometry of the cell features is illustrated. For example, if a minimum feature size is F .mu.m, then contact 402 may be approximately F.times.F .mu.m.sup.2, the length of second gate 324, interlayer dielectric 320, first gate 312, and tunnel dielectric 312 may be approximately 1.25 F, the length of **control gate** 322, interlayer dielectric 318, floating gate 314 and tunnel dielectric 310 may be approximately 1.5 F, the spacing between the two stacks of transistors may be approximately 1.25 F, and the length of floating gate 314 may be approximately 2.5 F to give a high **control gate to floating gate** coupling ratio. For this embodiment, with a feature size of 0.4 .mu.m, the cell size of EEPROM cell 300 may be from approximately 15 to 20 F.sup.2 or approximately 2.5 to 3.5 .mu.m.sup.2. For alternative embodiments, other feature sizes, line widths and lengths, contact sizes, and line spacing may be used.

Detailed Description Text - DETX (18):

A schematic representation of EEPROM 300 is illustrated in FIG. 12 in which **drain** region 308 is coupled to bit line 1202. EEPROM cell 300 may be programmed using programming voltages on the second and first gate of select transistor 328 that may be generally lower than those used by conventional EEPROM cells. This is due to the negative voltage applied to **control gate** 322 which consequently requires a smaller positive voltage on section 306. Programming and erasing of EEPROM cell 300 may be accomplished using

Fowler-Nordheim tunneling as summarized in Table 1 below.

Detailed Description Text - DETX (19):

Erasing a state stored on floating gate 314 may be accomplished by applying appropriate voltages to the terminals of floating gate transistor 326 such that floating gate 314 is at a much more positive potential compared to the inversion layer linking regions 306 and 304 formed due to the positive potential on layer 314. For example, select gate transistor 328 passes a zero or negative potential on 308 by applying a suitable bias on gate 316. Floating gate 314 may then be erased using Fowler-Nordheim tunneling by applying approximately 0 volts to region 304 (or allowing it to float), and approximately 15 to 18 volts to **control gate** 322. A high electric field may then be created across tunnel dielectric layer 310 such that electrons may flow from the channel region, region 306, and region 304, to floating gate 314. To reduce the positive voltage on **control gate** 322, a negative voltage may be applied to regions 308 and 302 as shown in Erase Scheme B in Table 1. Erase Scheme B may be used, for example, in a cell formed by the **triple-well** process shown in FIG. 3B. One or more EEPROM cells may be erased at the same time. It may take approximately 1 to 10 milliseconds (ms) to perform an erase function. This time may be amortized over the number or EEPROM cells that may be erased at one time.

Detailed Description Text - DETX (20):

Programming data or charge onto floating gate 314 may be accomplished by enabling select gate transistor 328 and applying appropriate voltages to the terminals of floating gate transistor 326. Select gate transistor 328 may be enabled by applying and approximately 4 to 7.0 volts on gates 324 and 316. Approximately 3 to 5.5 volts may then be applied to region 308 (bit line 1202) such that approximately 3 to 5.5 volts may be present at region 306. This range of voltages is significantly reduced relative to the higher voltages generally used by conventional EEPROM cells. Floating gate 314 may then be programmed using Fowler-Nordheim tunneling by floating region 304 and applying approximately -7 to -12 volts to **control gate** 314. A high electric field may then be created across tunnel dielectric layer 310 such that electrons may flow from floating gate 314 to **drain** region 306. One or more EEPROM cells (e.g., in the same row) may be programmed at the same time. It may take approximately 1 to 10 milliseconds (ms) to perform a program function. This time may be amortized over the number or EEPROM cells that may be programmed at one time.

Detailed Description Text - DETX (21):

EEPROM cell may be programmed using a small amount of current and a small amount of power. For one embodiment, EEPROM cell 300 may require from

approximately 10 nanoamperes (nA) of current to program EEPROM cell 300. Most of this current may flow from region 306 to region 302 due to band-to-band tunneling caused by high vertical fields on the tunnel dielectric. If the operating power supply is approximately 3 to 5 volts, then it may require approximately 30 nanoWatts (nW) to 50 nW to program EEPROM cell 300. The low programming current may be a result of the electron injection efficiency (i.e., the ratio of gate current to **drain** current injected into **drain** region 306) of using Fowler-Nordheim tunneling as opposed to other programming techniques such as hot electron injection. For one embodiment, the electron injection efficiency may be approximately 10.sup.-3 to 10.sup.-4.

Detailed Description Text - DETX (22):

Reading a state stored by floating gate 314 may be accomplished by enabling select gate transistor 328 and applying appropriate voltages to the terminals of floating gate transistor 326. Select gate transistor 328 may be enabled by applying approximately 2 to 5 volts on gates 324 and 316. Floating gate transistor 326 may then be biased such that approximately 0 volts are applied to region 304 and approximately 2 to 6 volts are applied to **control gate** 322. A voltage of approximately 1 to 2 volts may then be applied to region 308 (bit line 1202) and the state of floating gate transistor 326 sensed from bit line 1202.

Detailed Description Text - DETX (23):

FIG. 13 is a circuit diagram of one embodiment of an EEPROM cell array 1300 and circuitry for programming, erasing, and reading EEPROM cells in the array. EEPROM cell array 1300 may include EEPROM cells 1301 and 1302. EEPROM cells 1301 and 1302 may be formed in the same fashion as EEPROM cell 300 of FIG. 3A. For alternative embodiments, EEPROM cells 1301 and 1302 may be any other type of EEPROM cell. EEPROM cell 1301 may include a select transistor 1318 and floating gate transistor 1320. Select transistor 1318 may have a **drain** coupled to bit line 1316, a gate coupled low voltage decoder 1310, and a **source** coupled to the **drain of floating gate** transistor 1320. The gate of select transistor 1318 may be formed from two layers of conductive gate material as in EEPROM cell 300 of FIG. 3A. Floating gate transistor 1320 may include a **control gate** coupled control logic 1304 via line 1326, a floating gate 1319, and a **source** coupled to line 1322. EEPROM cell 1302 may include a select transistor 1306 and floating gate transistor 1308. Select transistor 1306 may have the **drain** coupled to bit line 1316, a gate coupled low voltage decoder 1312, and a **source** coupled to a **drain of floating gate** transistor 1308. The gate of select transistor 1306 may be formed from two layers of conductive gate material as in EEPROM cell 300 of FIG. 3A. Floating gate transistor 1308 may include a **control gate** coupled control logic 1304 via line 1326, a floating gate 1307,